

Applicant(s): Matthew J. Adiletta et al.

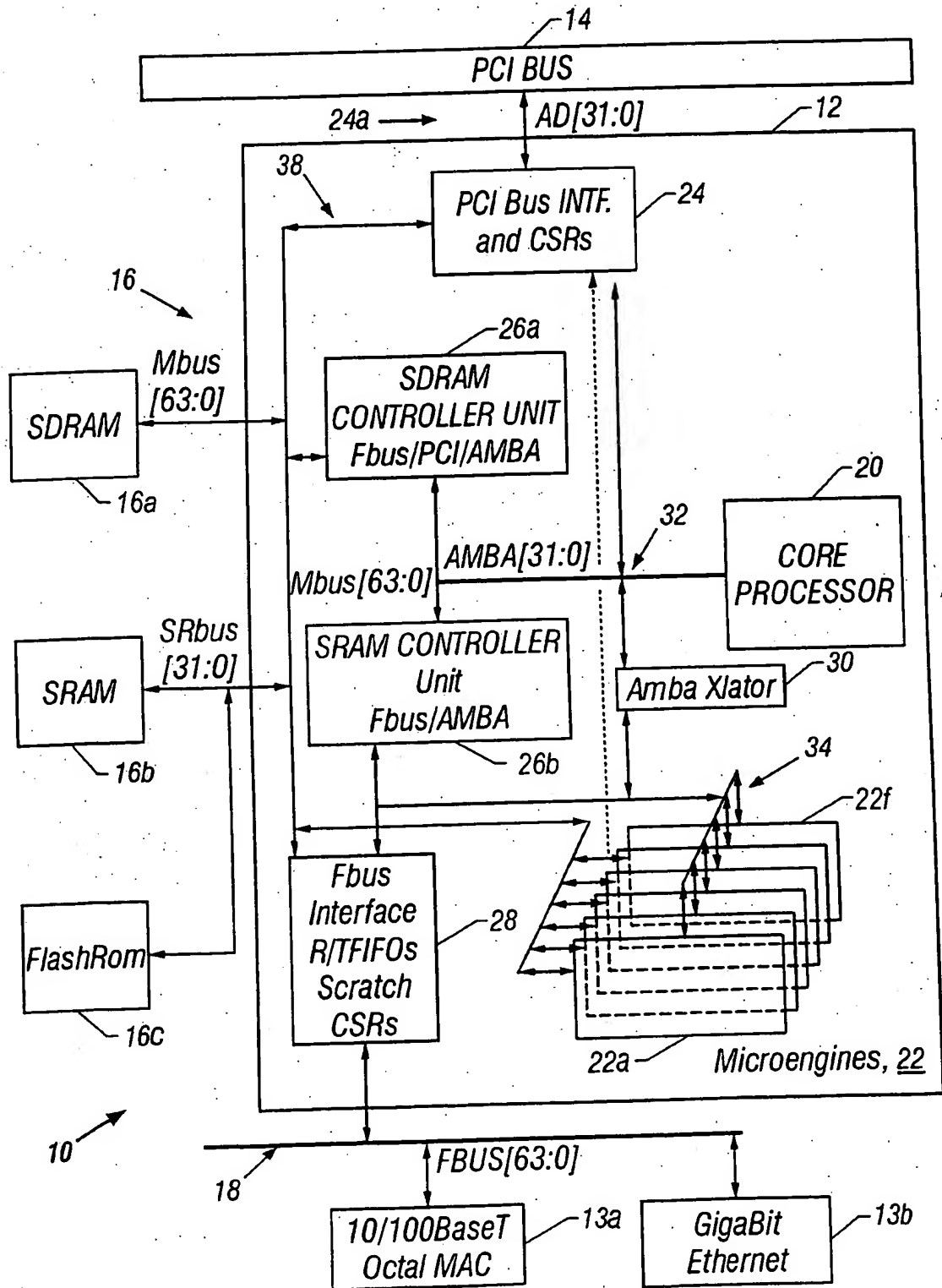
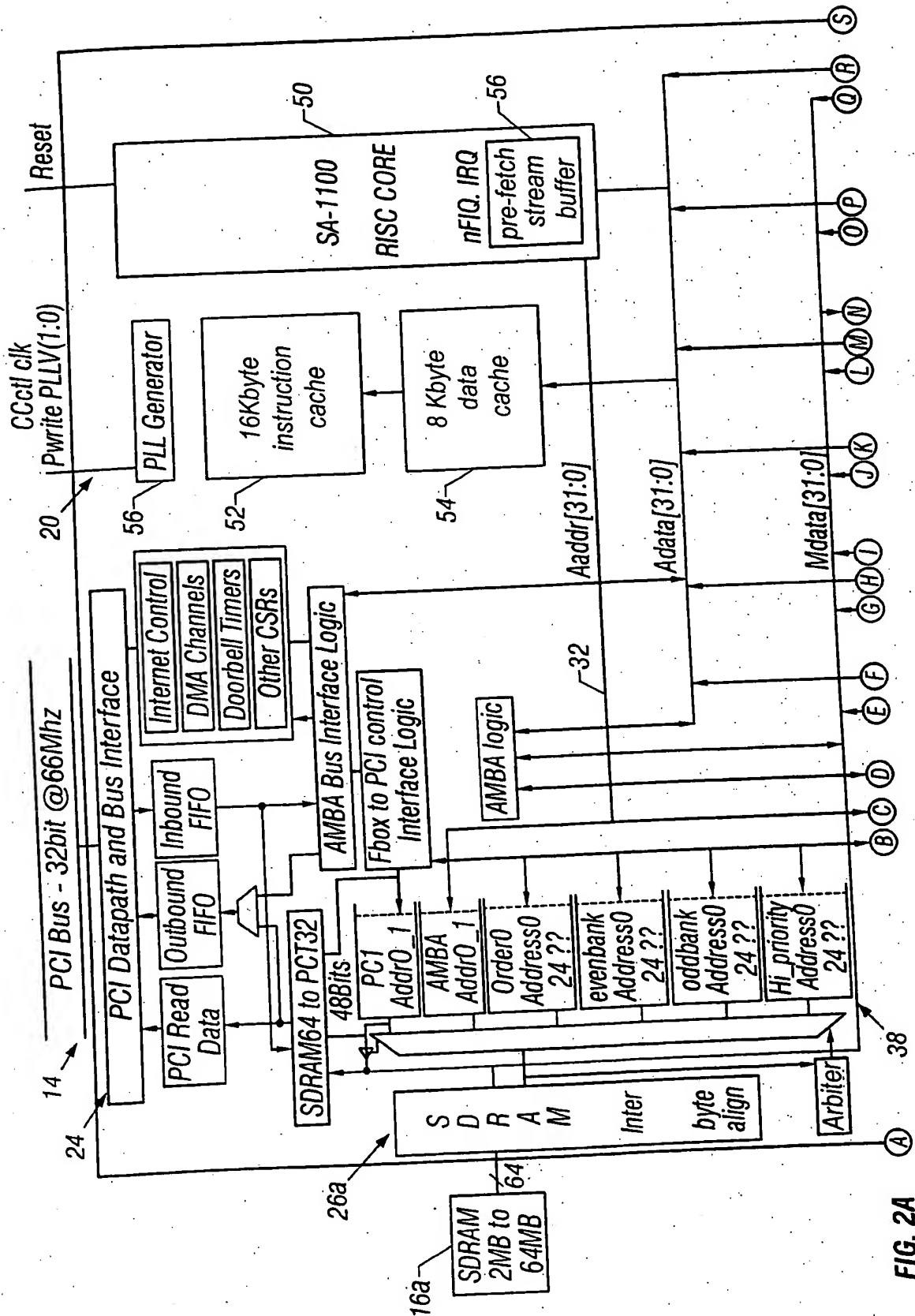
SRAM CONTROLLER FOR PARALLEL PROCESSOR
ARCHITECTURE INCLUDING AN ADDRESS AND COMMAND
QUEUE AND METHOD FOR CONTROLLING ACCESS TO A
RAM

FIG. 1



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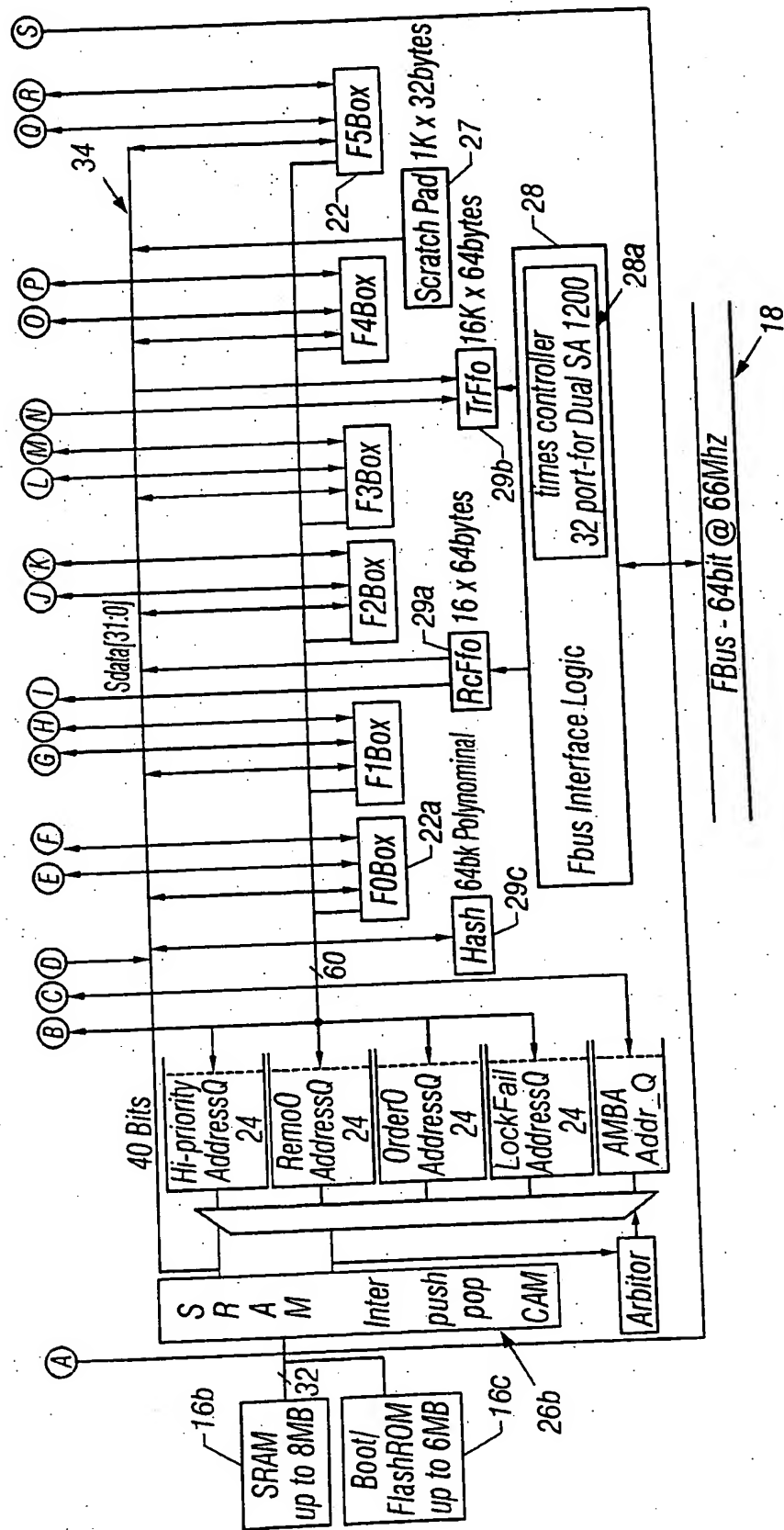


FIG. 2B

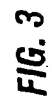
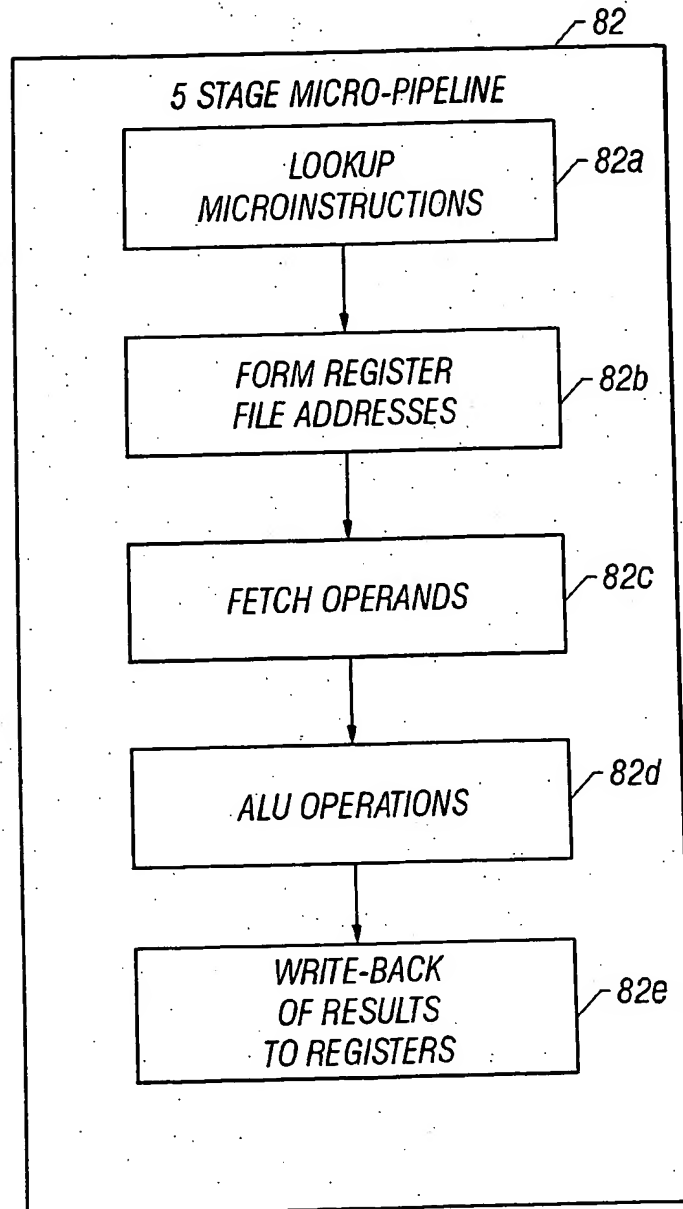


FIG. 3

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SRAM CONTROLLER FOR PARALLEL PROCESSOR
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```

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+
CONTEXT | 1 | 1 | 1 | 1 | xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx | 1 | 0 | db | xx | wake-up event | va | xxxxxxxx | ctx cmd |
+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+---+

```

Context Descriptors:

1) Wake-up Events (Bits 8-15)

- 0 = kill
- 1 = voluntary
- 2 = SRAM
- 4 = SDRAM
- 8 = FBI
- 16 = INTER_THREAD
- 32 = PCI_DMA_1
- 64 = PCI_DMA_2
- 128 = SEQ_NUM_LSB

- 2) db -> branch defer amount (Bit 17)
- 3) va -> value of sequence number (Bit 7)
- 4) OPCODE Bits (29-31)
- 5) cxt_cmd

FIG. 3B

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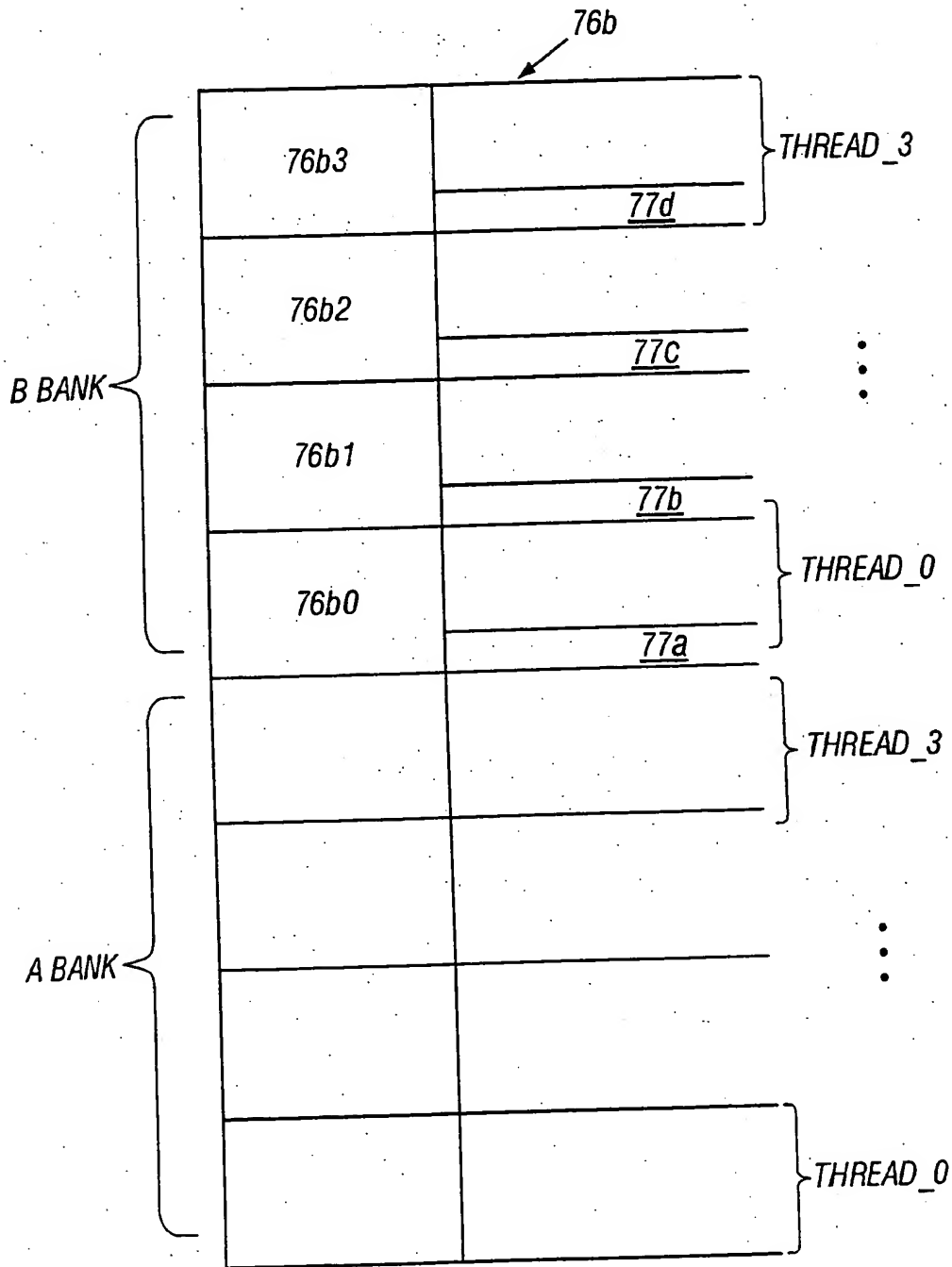
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FIG. 3C



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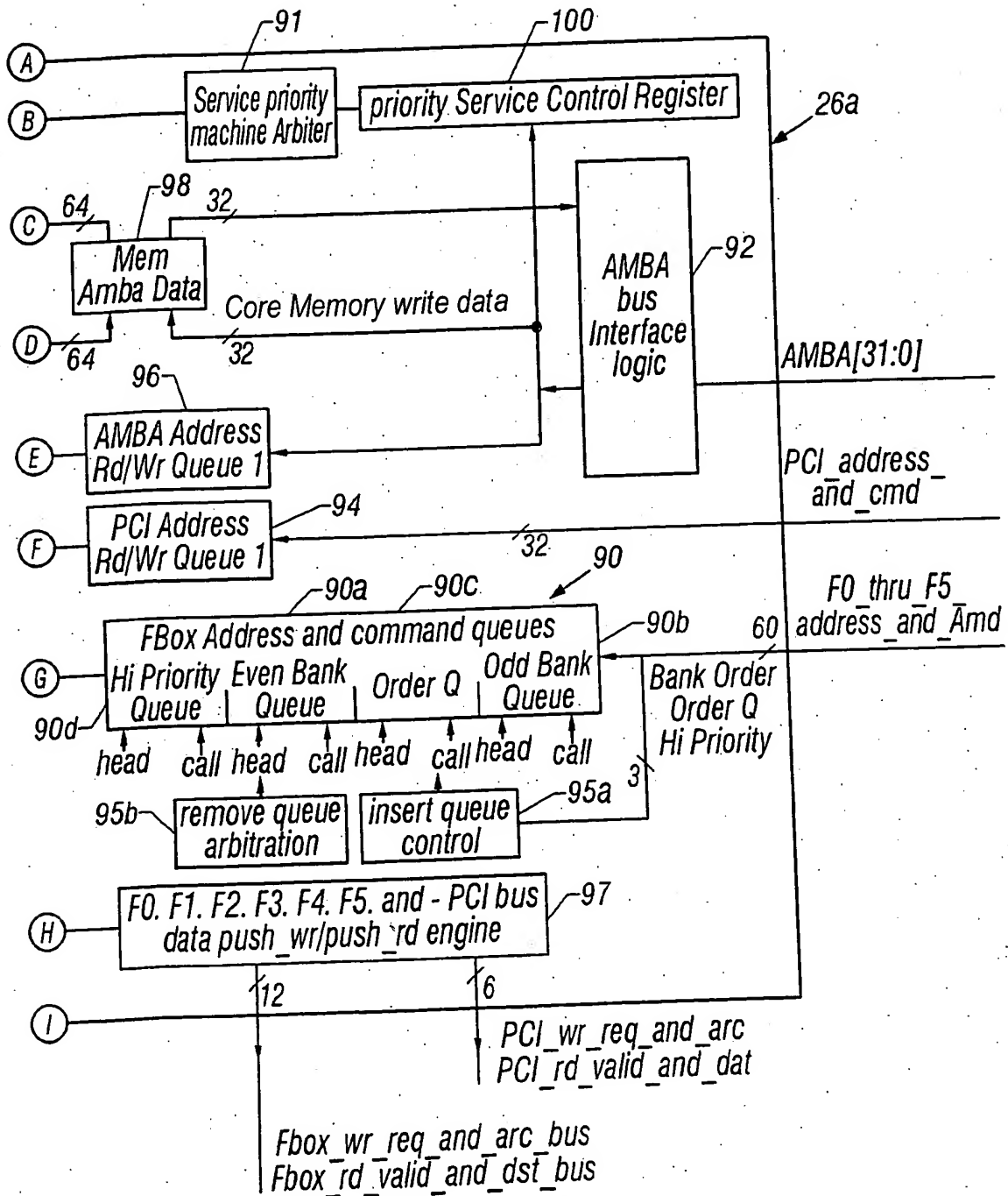


FIG. 4B

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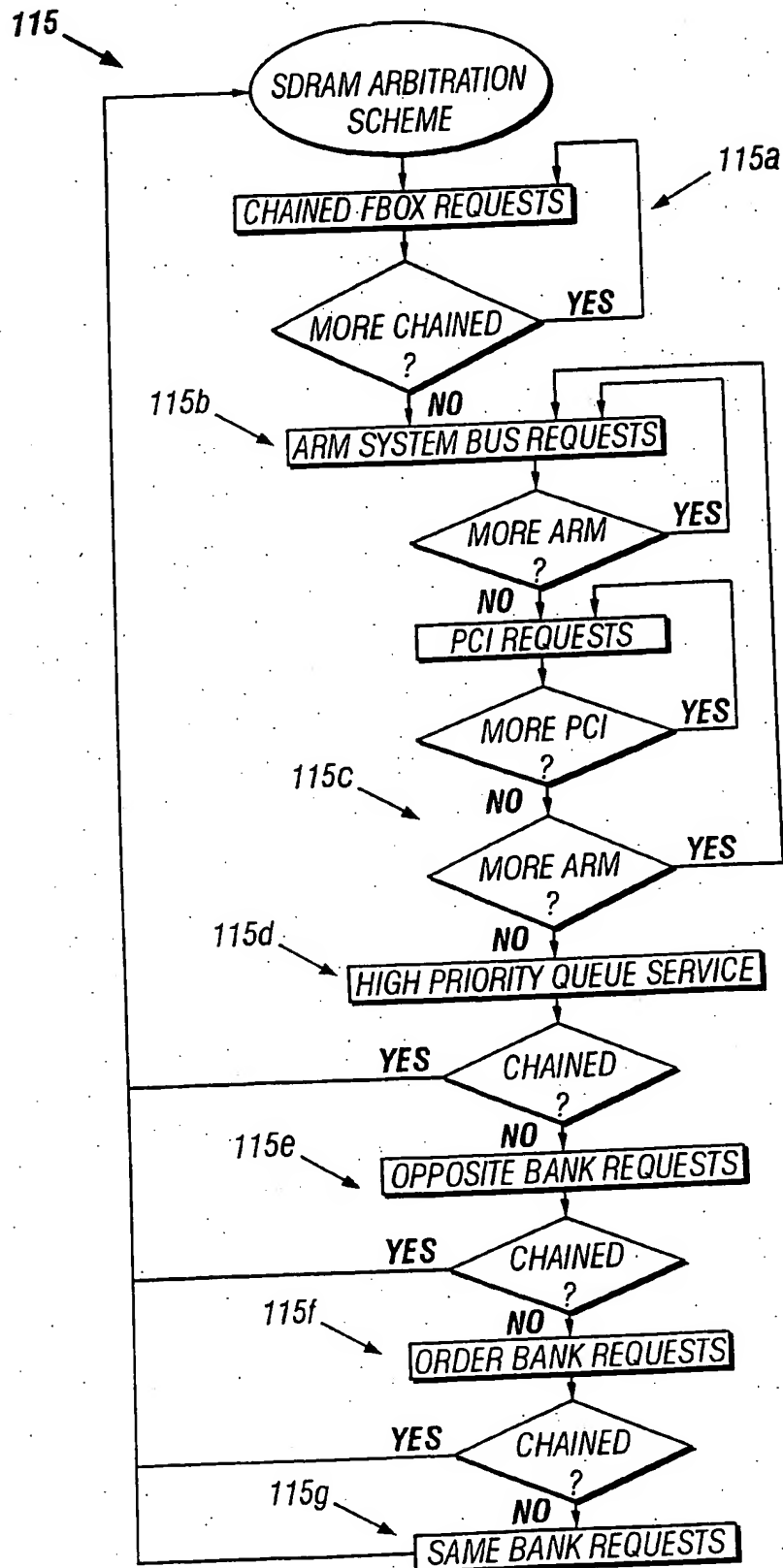


FIG. 4C

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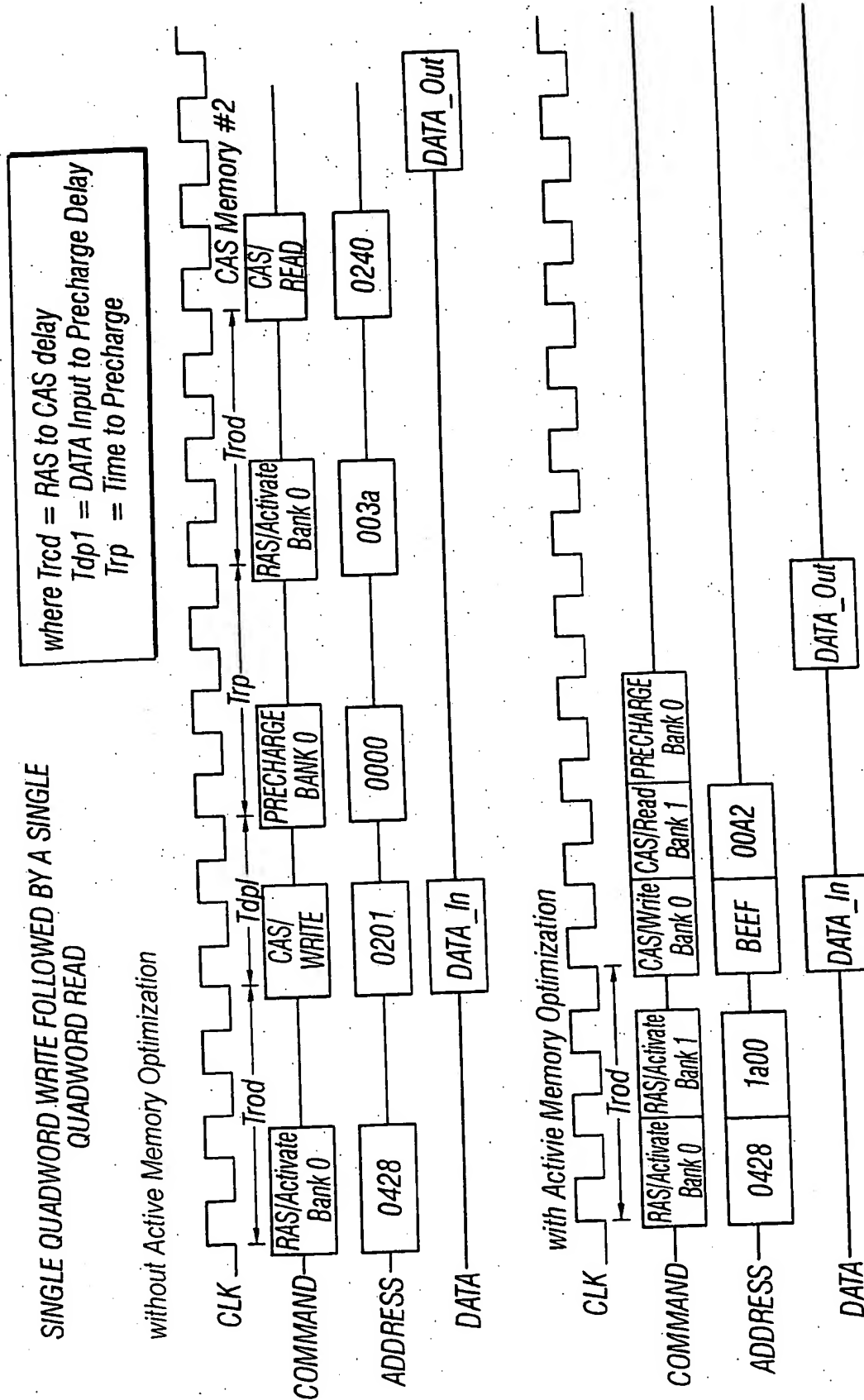
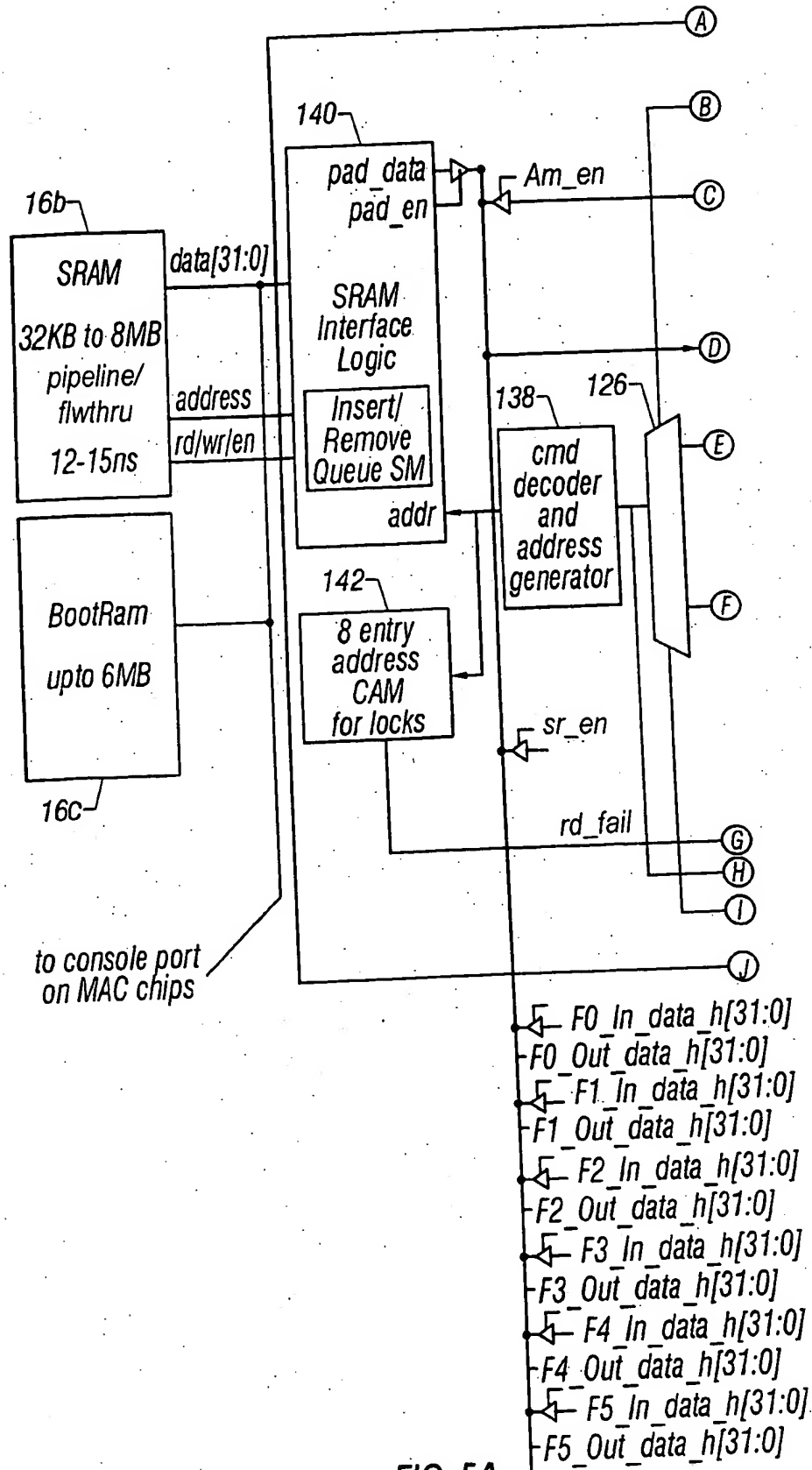


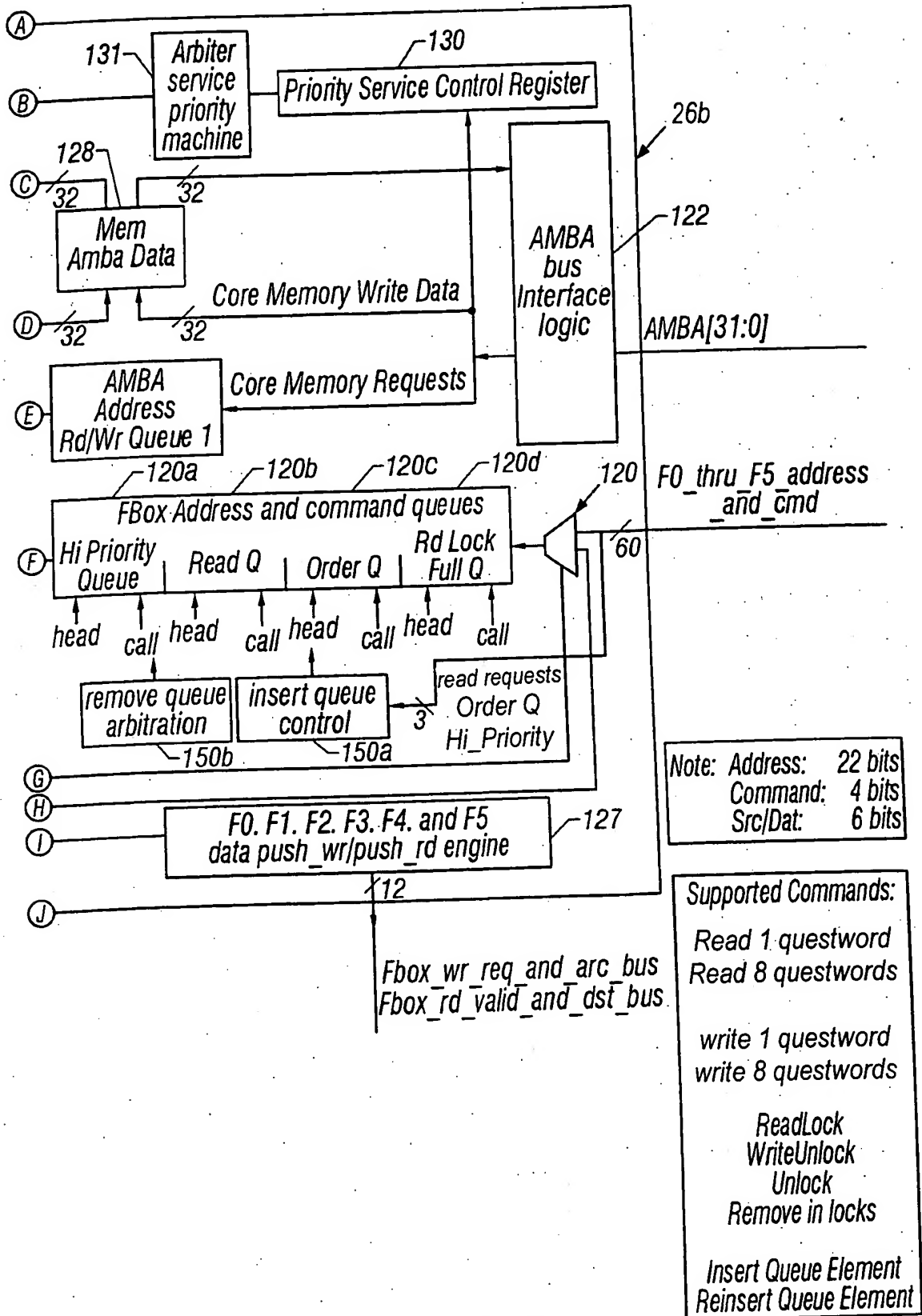
FIG. 4D

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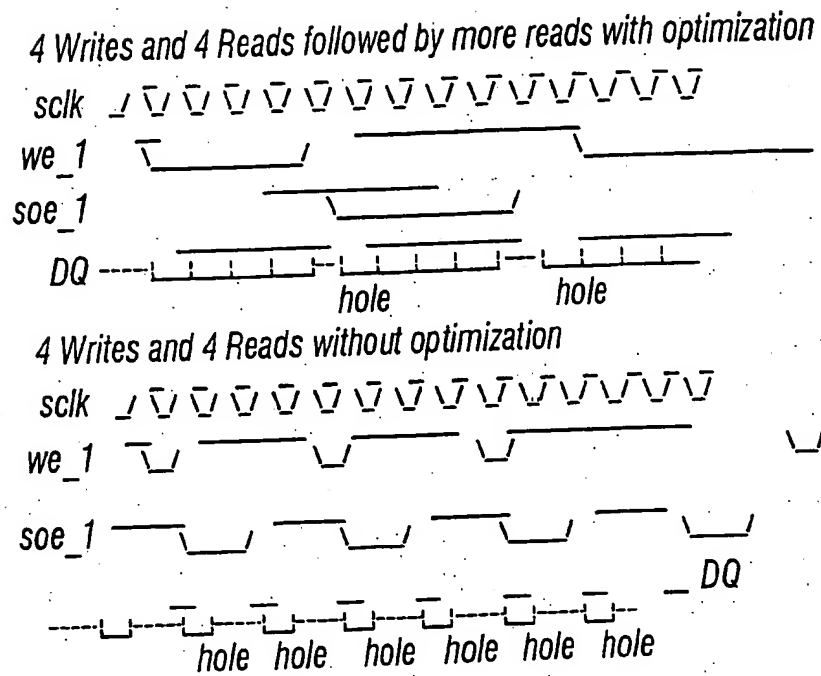


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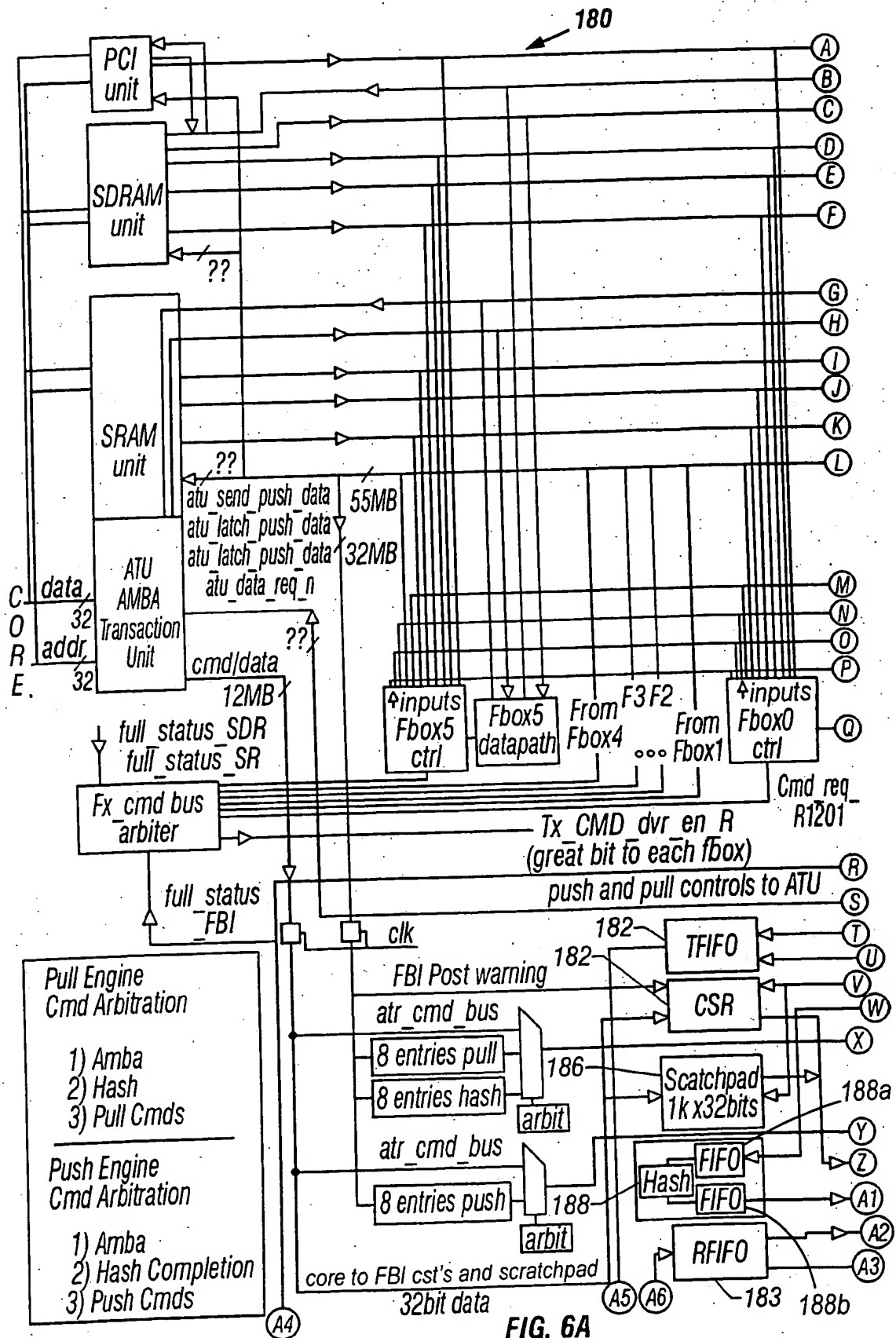


FIG. 6A

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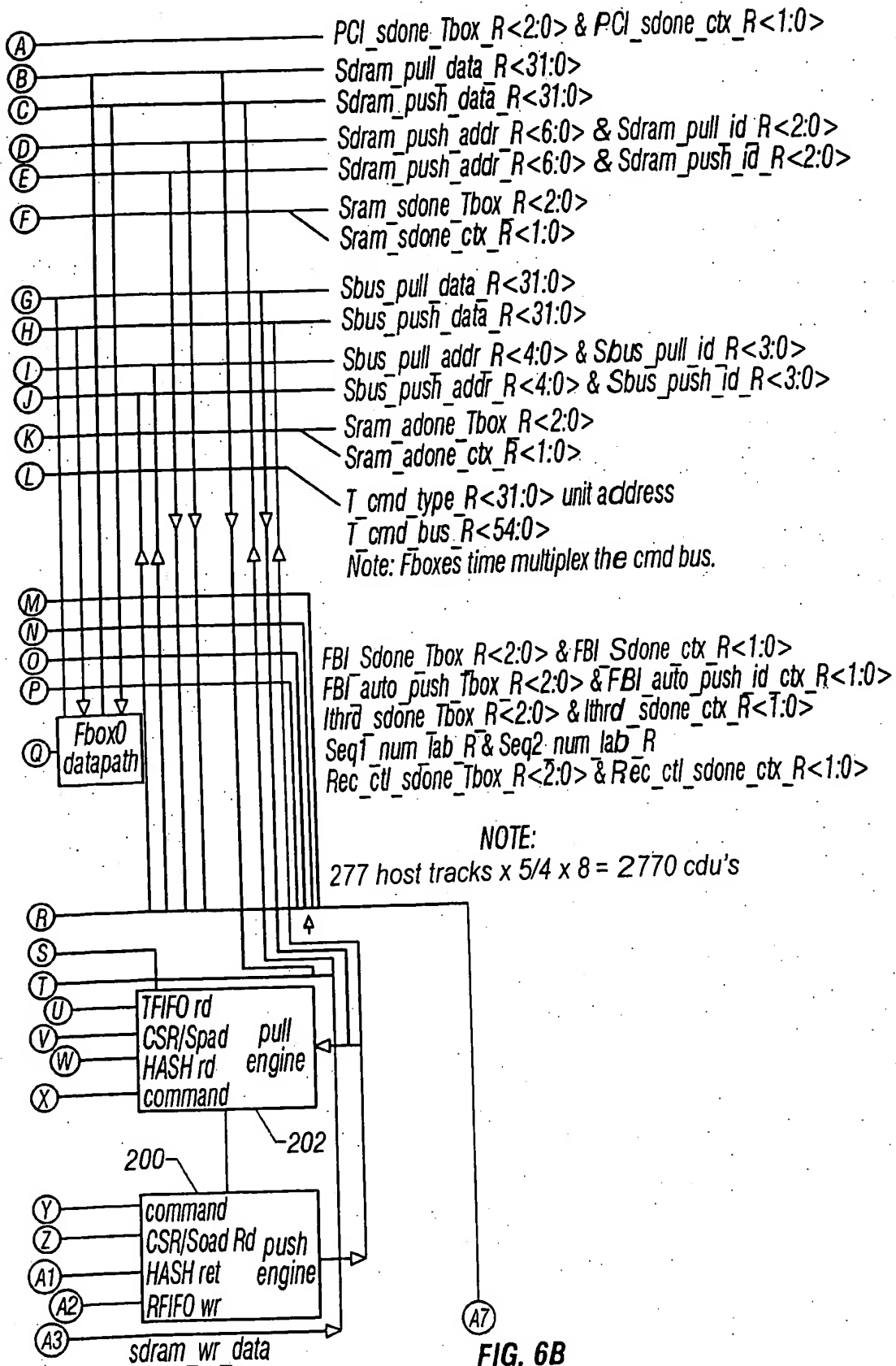


FIG. 6B

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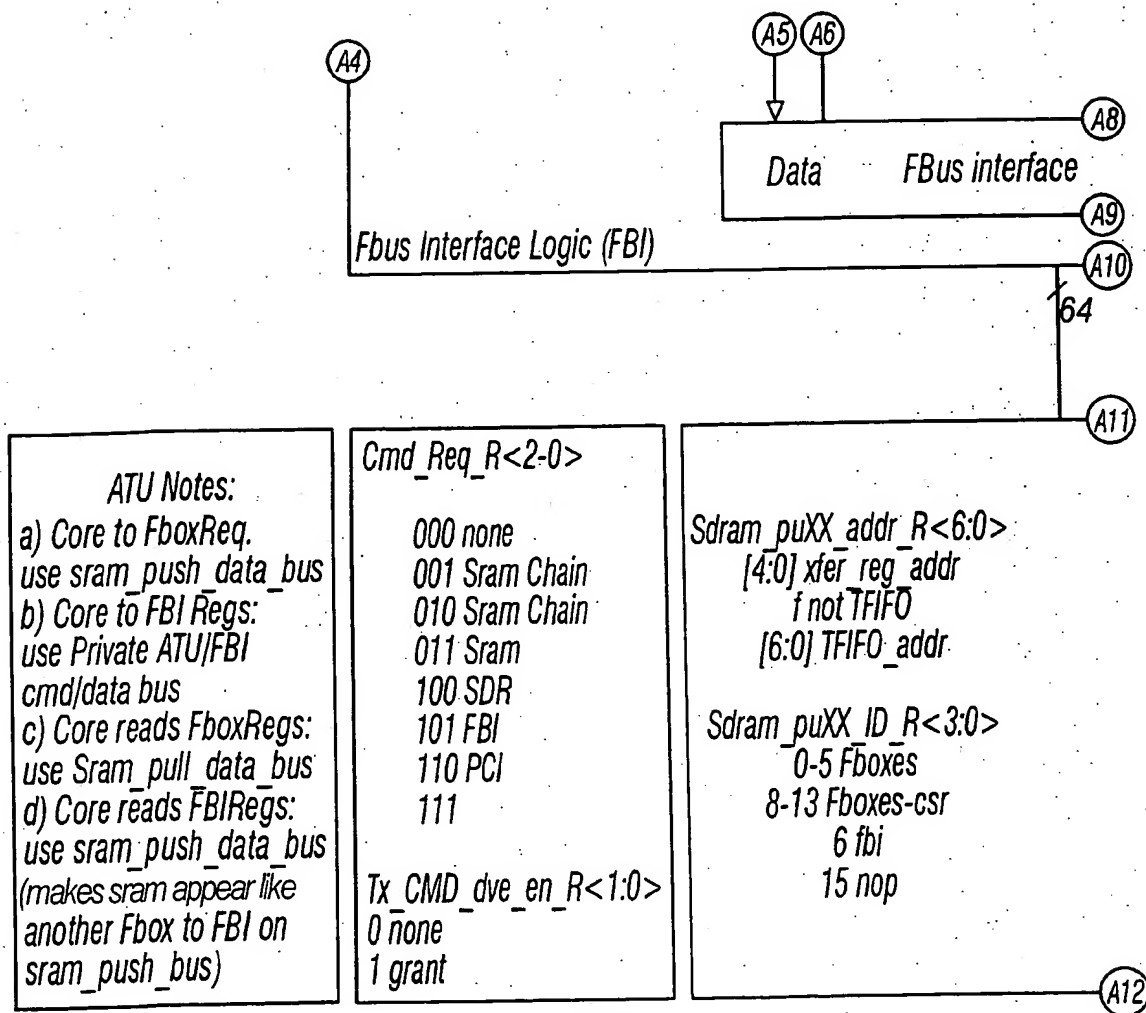


FIG. 6C

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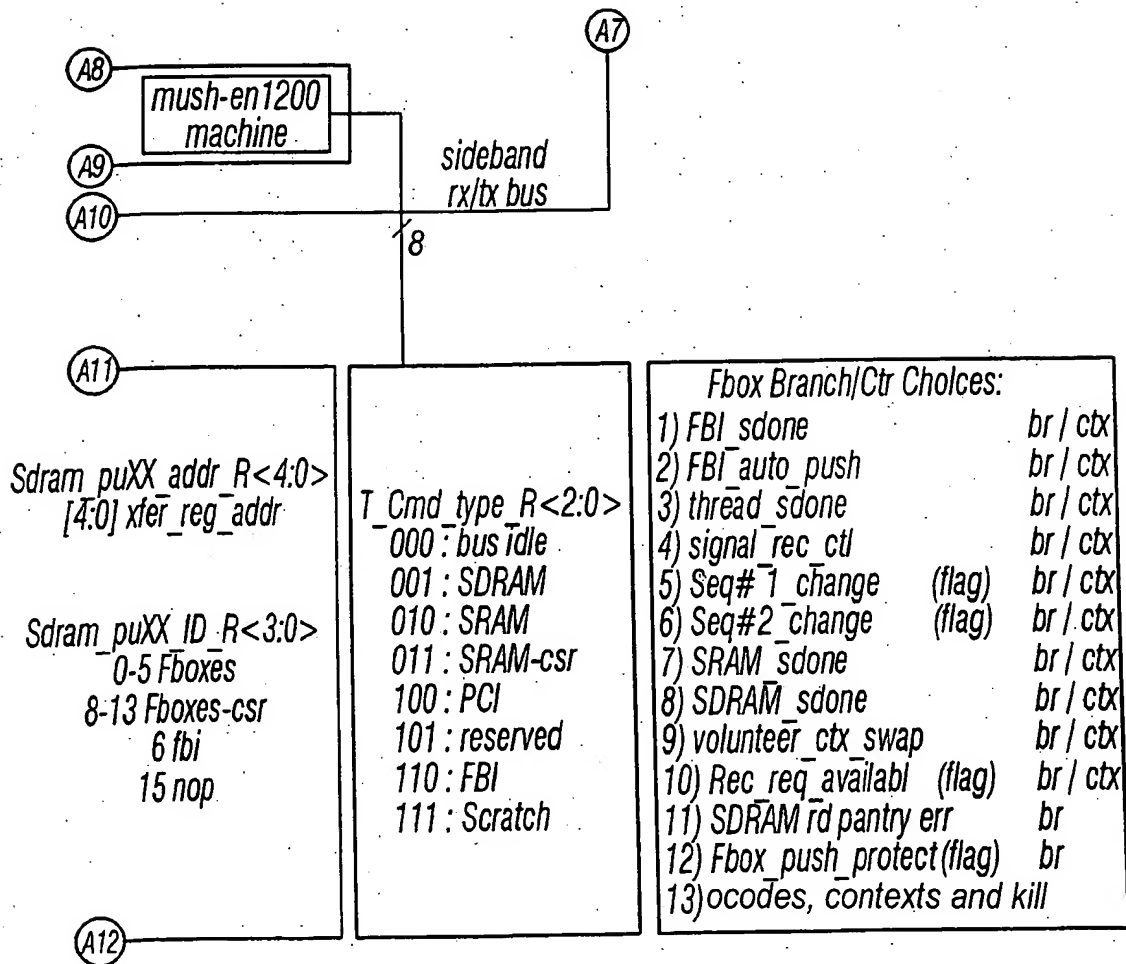


FIG. 6D